TEMPERATURE CHARACTERISTICS OF GAA SINWFET'S TRANSISTOR STRUCTURES

The results of numerical simulation by Silvaco TCAD [1] of 3D FET-transistors with five n-type of conductivity Si-nanowires (n-SiNW FET’s) 5-channels, based on Gate-all-around (GAA) structure are presented. Among them except the possibility of further nanoscale procedure, GAA n-SiNW FET’s have an excellent gate controlling, short-channel effects (SCE’s) stability [2-6], etc. It is demonstrated their distinct electrical characteristics, in particular there were obtained the valid values of threshold voltage \( V_t \), leakage current \( I_{off} \) and \( I_{on}/I_{off} \) coefficient, subthreshold scattering \( SS \) and drain induced barrier lowering (DIBL). At fixed drain voltage 1.2 V a further temperature increasing in the range 280-400 K leads to decreasing the threshold voltage \( V_t \) on 21.9 %, to increasing the subthreshold scattering \( SS \) on 43.6 %, to «switch-on» current decreasing on 11.2 % and to DIBL decreasing on 7.3 %.

### Table 1

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Working temperature</th>
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<tbody>
<tr>
<td>( V_t ), V</td>
<td>280K 300K 320K 340K 360K 380K 400K</td>
</tr>
<tr>
<td>SS, mV/decade</td>
<td>59.7 65.3 68.3 72.6 76.9 81.3 85.7</td>
</tr>
<tr>
<td>( I_{off} \times 10^{12} ), A</td>
<td>0.08 0.40 1.61 5.54 16.73 45.34 111.9</td>
</tr>
<tr>
<td>( I_{on} \times 10^6 ), A</td>
<td>10.83 10.61 10.41 10.21 10.01 9.86 9.62</td>
</tr>
<tr>
<td>( (I_{on}/I_{off}) \times 10^{-6} )</td>
<td>135.3 26.52 6.47 1.84 0.60 0.22 0.09</td>
</tr>
</tbody>
</table>

5-channel GAA SiNW FET working characteristics at “drain-source” voltage values of \( V_{DS} = 1.2 \) V are presented in Table 1. It should be noted, that at room temperature (\( T = 300 \) K) \( V_t \) and SS values were 0.40 V and 65.3 mV/decade, respectively. Currents \( I_{on}, I_{off} \) and \( I_{on}/I_{off} \) coefficient values were 10.61 \( \times 10^6 \) A, 0.40 \( \times 10^{-12} \) A and 26.5 \( \times 10^6 \) a.u., respectively. Calculation of the DIBL values at fixed temperatures of 280 K and 400 K has been shown its negligible decreasing from 35.7 mV/V to 33.1 mV/V.

The GAA SINWFET’s temperature dependences of work characteristics are determined by the temperature dependence of the mobility of charge carriers in the semiconductor, the redistribution of charge carriers by energy and the Fermi level shift, the temperature dependence of the dielectric separating the gate from the channel. In particular, with increasing temperature, the mobility in the semiconductor decreases, which causes an increase in the resistance of the channel and the current drop through it. Along with this, the redistribution of charge carriers by energies and
the shift of the Fermi level of the semiconductor leads to the fact that the induced channel is formed near the surface of the semiconductor under the gate at lower electric field strength, i.e., at lower threshold voltage [5, 6]. With increasing temperature there is a significant increase in the leakage current of the transistor gate (see the corresponding line for the value $I_{0}$ in Table 1).

For measurement the electrical characteristics of 5-channel GAA n-SiNWFET’s there were designed the corresponding structures with the channels lengths of 30 nm and a Si-nanowires thickness $T_{FIN} = 8$ nm and height $H_{FIN} = 8$ nm, their geometry is presented on Fig.1a. 3D transistors had a gate length of $L_G = 14$ nm, the work function of gate electrode (TiN) due to was 4.40 eV ($n$-type of conductivity). During the structures designing it was used the following channels optimal doping profiles configuration in channel’s volume the concentration of acceptor impurity was $5 \times 10^{15}$ cm$^{-3}$ and in near-contact Al (drain and source) areas it was doped a donor impurity with higher concentration of $5 \times 10^{18}$ cm$^{-3}$. As a high-k isolator was used HfO$_2$ (k=22) which had a thickness 2 nm, a corresponding barrier layer SiO$_2$ under high-k isolator had a thickness 1 nm.

![Materials](image1.png)

![Fig. 1. Structures of 5-channel GAA n-SiNW FET’s (a) and $I_{DS}$-$V_{GS}$ curves (b) as a function of temperature variations and fixed “drain-source” voltage values of 1.2 V and 0.1 V](image2.png)

A typical $I_{DS}$-$V_{GS}$ dependencies at temperatures of 300, 340 and 380 K for proposed GAA n-SiNWFET’s structures with in case of fixed drain-source voltage values of $V_{DS} = 1.2$ V and $V_{DS} = 0.1$ V are presented on Fig. 1b. As the temperature increases, the steepness (slope) of the characteristic decreases, and the threshold voltage $V_{T}$ decreases, and there is a point (thermostable point) at which the opposite effects are compensated and the current through the channel (drain current) remains unchanged. In case of proposed structures a position of this point is situated close to the following values: $I_{DS}=5.1 \times 10^{-6}$ A, $V_{GS} = 0.53$ V ($V_{DS} = 0.1$ V) and $I_{DS}=9.6 \times 10^{-6}$ A, $V_{GS} = 0.68$ V ($V_{DS} = 1.2$ V).

**Conclusions:** GAA SiNWFET’s with 5 channels doped by acceptor impurity with concentration of $5 \times 10^{15}$ cm$^{-3}$, have been successfully designed and studied the influence of the working temperatures of 280 - 400 K on static transmission and other working characteristics. There were obtained typical temperature dependencies. Their view may be caused by the well-known fundamental theories in case of nanotransistors [5, 6].
References:


